ENGINEERING AND TECHNOLOGY GROUP

ELECTRONICS TECHNOLOGY

Scheme of Examination
Std. XI

Paper	Title of the Paper	Theory		Practical		Term work	Project work	I.V.*	Total Marks
		Marks	Time (Hrs)	Marks	Time (Hrs)				
3	Digital Electronics	80	3	80	3	20	10	10	200

* IV = Industrial Visits

Paper III: Digital Electronics

Sr. No.	Unit	Sub-unit	Periods
1.	Number Systems and Binary Arithmetic	1.1 Number Systems and conversions	12
		1.2 Binary Arithmetic	
		1.3 Codes	
2.	Logic Gates	2.1 Basic Gate	15
		2.2 Derived Gates	
		2.3 Boolean Algebra	
		2.4 Applications of Ex-OR gate	
3.	Logic Families	3.1 Introduction of Logic Families	10
		3.2 TTL Logic Circuits	
		3.3 CMOS Logic Circuits	
4.	Combinational Logic Circuits	4.1 Multiplexer	20
		4.2 De multiplexer	
		4.3 Encoder	
		4.4 Decoder	
5.	Flip-flops	5.1 Introduction to Flip-flop	20
		5.2 S-R flip flop	
		5.3 D flip flop	
		5.4 J-K Flip flop	
		5.5 JK-MS	
		5.6 T Flip flop	

6.	Registers	6.1 Introduction and types of register	10
		6.2 Left shift register	
		6.3 Right shift register	
7.	Counters	7.1 Types of counters	21
		7.2 Ripple counter	
		7.3 Decade counter	
		7.4 Down counter	
		7.5 Up/down counter	
		7.6 Ring counter	
8.	Data conversion	8.1 Need of Data conversion	12
		8.2 DAC	
		8.3 ADC	
Total			**120**